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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/521,280	03/07/2000	Stephan Voges	EFIM0252	9230

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EXAMINER
KISS, ERIC B

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 09/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/521,280	VOGES ET AL.	
	Examiner	Art Unit	
	Eric B. Kiss	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-54* is/are rejected.

7)☒ Claim(s) *21 and 49* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03/07/2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-54 have been examined.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "10", "20", "100", "110", and "120" in Fig. 1.

Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect may be deferred until after the examiner has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.

Specification

3. The disclosure is objected to because of the following informalities:

In the section describing the $tclSetMCD and $tclAddMCD functions (page 19, lines 6-16), there is no clear definition of what portion of the described method corresponds to each function.

The use of the trademark VERILOG has been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

Appropriate correction is required.

Claim Objections

4. Claims 21 and 49 are objected to because of the following informalities: Claim 21 recites the limitation "under a predefined conditions" on page 29, line 3. The word "conditions" should be made singular to agree with the singular article "a".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 18, 22-26, 29, 46, 50, 51 and 53 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 18 and 46 recite the limitation "without any connection to Verilog" in the description of the $tclShareVariables function. Since this claimed function is part of the TCL_PLI library apparently expressly designed for interaction between Tcl and Verilog, wherein the general scope of the specification encompasses using Tcl as a scripting interface for Verilog, there does not appear to be any support for this claimed limitation.

Claims 22 and 50 recite the limitation "Synopsys LMC source models" which is merely restated from the preferred embodiment description (page 20, line 20) and not defined therein.

Claims 23-26 and 51 are drawn to the portion of the specification regarding the "Synopsys LMC source models" as mentioned above, wherein the method and apparatus components claimed depend on the use of the source models.

Claims 29 and 53 recite the limitations of "providing a porting of Tcl scripts to real hardware" and "running a verification suite on ASICs when they return from a foundry" which is merely restated from an alternative embodiment description that provides no further enabling disclosure.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-29 and 31-54 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The claims are generally indefinite, failing to conform with current U.S. practice. They are replete with 35 U.S.C. 112, second paragraph problems such as lack of antecedent basis. The claims should be revised carefully in order to comply with 35 U.S.C. 112, second paragraph. In light of this, a lack of a rejection based on prior art to a particular claim should not be construed as an indication of impending allowability of that claim.

b. Claim 1, on lines 13 and 16, recites the limitation "said task". There is insufficient antecedent basis for this limitation in the claim. A previous recitation of the plural "tasks" can be found on line 10. It is unclear whether a single task or a plurality of tasks is intended. In the interest of compact prosecution, occurrences of "task" and "tasks" in claim 1 are treated as reading "one or more tasks" for subsequent examination on the merits. This treatment addresses some antecedent basis problems in subsequent dependent claims (see, for example, "said one or more verification engine tasks" in claim 9).

c. Claim 1, in lines 10-11, recites the limitation "wherein said simulation starts up an interpreter and instructs it to run a script" following a recitation of "one or more interpreters". It is unclear whether the simulation starts up only one interpreter and subsequently only one script or whether plurality is intended. In the interest of compact prosecution, the claim is treated as reading "wherein said simulation starts up said one or more interpreters and instructs each of said one or more interpreters to run a script" for subsequent examination on the merits. This treatment addresses some antecedent basis problems in subsequent dependent claims (see, for example, "said one or more scripts" in claim 21).

d. Claim 18, in lines 9 and 11, recites the limitation "said $tclShareVariables function". There is insufficient antecedent basis for this limitation in the claim.

e. Claim 24, on line 2, recites the limitation "said Tcl interpreters". There is insufficient antecedent basis for this limitation in the claim. In the interest of compact prosecution, the claim is treated as reading "said interpreters" for subsequent examination on the merits.

f.. Claim 26 recites a functional negative step that is not a natural result of previous steps.

g. Claim 54 is not clearly and positively recited. Use of the word "may" renders the claim indefinite because it is unclear whether the limitation(s) following the word are part of the claimed invention. See MPEP § 2173.05(d).

h. Claim 4, 13-15, 18-20, 24, 26, 28, 34, 41-43, 46-48, and 51 contain the trademark/trade name Verilog. Where a trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of 35 U.S.C. 112, second paragraph. See *Ex parte Simpson*, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. A trademark or trade name is used to identify a source of goods, and not the goods themselves. Thus, a trademark or trade name does not identify or describe the goods associated with the trademark or trade name. In the present case, the

trademark/trade name is used to identify/describe a particular verification engine product and, accordingly, the identification/description is indefinite. Subsequently, Verilog is interpreted as referring to the description set forth in IEEE Standard 1364-1995 "IEEE standard hardware description language based on the Verilog hardware description language" and later revised in IEEE Standard 1364-2001 "IEEE standard Verilog hardware description language".

i. Claims 31-54 recite the limitation "The apparatus of claim 29" either explicitly or implicitly due to dependencies. There is insufficient antecedent basis for this limitation in the claims as claim 29 is a method claim and not an apparatus claim. Claims 31-54 appear to contain other severe dependency numbering problems resulting in numerous antecedent basis problems.

Since claims 31-53 otherwise appear to be apparatus versions paralleling the method claims 1-7, 10-22, 26, 27, and 29, respectively, and recite no additional significant limitations, they are treated as such, adopting a dependency structure with claim 30 as the top-level claim, paralleling that of claims 1-7, 10-22, 26, 27, and 29. This treating is applied in the interest of compact prosecution for subsequent examination of claims 31-53. Consequently, all 35 U.S.C. 112, second paragraph rejections applied above to claims 1-7, 10-22, 26, 27, and 29 also apply to claims 31-53, respectively.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1, 2, 4-10, 30, 31, 32, 34-38, and 54 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,600,579 to Steinmetz, Jr. (hereinafter Steinmetz).

As per claims 1, 30, and 31, Steinmetz teaches a method and system for partitioning functionality of a test bench (hardware design verification system) between a design verification engine (simulator means) and a scripting language (scripting means; see column 3, lines 3-19 and Fig. 1). Steinmetz further teaches instantiating an interpreter (dispatch module) in one or more test benches or simulations through a library of one or more scripted routines, the interpreter (dispatch module) causing tasks to be executed, and the interpreter running a script (see column 8, line 13 through column 9, line 22). Steinmetz further teaches passing control to the verification engine (master module) for execution of a verification engine task encountered in the script and resuming execution of the script after executing the verification engine task (see column 11, line 52 through column 12, line 4).

As per claims 2 and 32, Steinmetz further teaches passing control between the verification engine and a scripted routine through a function call for execution of a verification engine task and resuming execution of the script after executing the verification engine task (see column 23, lines 30-39). Steinmetz further teaches the verification engine controlling when an interpreter is invoked (see column 24, lines 15-18).

As per claims 4 and 34, Steinmetz further teaches using a Verilog engine (see column 22, lines 10-17).

As per claims 5 and 35, Steinmetz further teaches synchronizing the simulation and interpreter using a semaphore (acknowledgement command word; see column 23, lines 30-39).

As per claims 6 and 36, Steinmetz further teaches providing a verification engine module (example Verilog master model) for determining when an interpreter is invoked and causing verification engine tasks to be executed (see column 23, line 57 through column 25, line 10; in particular, see column 24, lines 22 and 23 for determining when an interpreter is invoked).

As per claims 7 and 37, Steinmetz further teaches a function call executing a script (forking the script; see column 7, lines 32-40), a coded function call executing a verification engine task (verification system library routines; see column 19, lines 45-58), and a function call resuming script execution (returning an acknowledgement command word; see column 23, lines 33-39).

As per claim 8, Steinmetz further teaches a verification engine task having access to arguments passed to an interpreter function that invoked the task (see example test script, column 20, line 41 through column 22, line 8). The example test script contains, for example, a WrtWrd command (column 21, lines 59-60) that contains as arguments a memory address to write data to and the actual data to be written. The verification engine task has access to these arguments through the command word sent by the interpreter (see column 21, lines 5-15).

As per claim 9, Steinmetz further teaches a verification engine task controlling return values of a corresponding interpreter (see example test script, column 20, line 41 through column

22, line 8). The example test script contains, for example, a RdWrd command (column 21, lines 61-62) that receives as a return value data read by a verification engine task.

As per claims 10 and 38, Steinmetz further teaches providing routines for direct sharing of information between an interpreter and a verification engine (see WrtWrd and RdWrd commands as described above pertaining to claims 8 and 9) and between different interpreters (streams; see column 8, lines 13-38).

As per claim 54, Steinmetz teaches a plurality of scripts (tests) in the process of execution, running in parallel (see column 25, line 57 through column 26, line 7).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 3, 11, 21, 27, 28, 33, 39, 49, and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steinmetz as applied to claims 1 and 30 above and further in view of the ModelSim Version 5.1 software product as described in "ModelSim EE/PLUS User's Manual: VHDL, Verilog, and Mixed-HDL Simulation for Workstations Version 5.1," published in 1997 (hereinafter ModelSim).

As per claims 3, 11, 27, and 28, Steinmetz discloses with such a C language scripting method and library for use with the script and the PLI and further teaches reuse of scripts in system level testing (see column 25, lines 49-56), but fails to disclose a Tcl language scripting method and library. However, ModelSim teaches the use of the known Tcl interpreted scripting language within a Verilog simulation environment as an aid to rapid development (see page 481 and the first paragraph under "Tcl examples" on page 488). Therefore, it would have been obvious to one having ordinary skill in the computer art at the time the invention was made to modify the C language scripting method and library of Steinmetz to use the known Tcl scripting language as taught by ModelSim. One would be motivated to do so to gain the advantage of rapid development and limited recompiling that Tcl provides as was once taught by ModelSim.

As per claim 21, ModelSim further teaches printing (returning) a warning message under a predefined condition (less than n matches found by the up/down command (see bottom of page 275). Therefore, it would have been obvious to one having ordinary skill in the computer art at the time the invention was made to further modify the Steinmetz method to include displaying warning messages as once taught by ModelSim. One would be motivated to do so to allow reporting of an unexpected return value of a function.

As per claims 33, 39, 49, and 52, these are apparatus versions of the claimed methods discussed above (claims 3, 11, 21, and 27, respectively), wherein all claim limitations also have been addressed as set forth above. Thus, accordingly such claims also would have been obvious.

13. Claims 12-17 and 40-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steinmetz in view of ModelSim as applied to claim 11 above, and further in view of "Tcl Built-In Commands – interp manual page" by Critchlow, Jr. (hereinafter Interp Manual).

As per claims 12 and 13, ModelSim further teaches using Tcl to create custom functions for interaction with Verilog tasks (see the last sentence on page 481). ModelSim further teaches a function (alias; see page 246) that defines new Tcl functions that are used to invoke Verilog tasks, maps the functions to specific tasks (commands), and defines how many arguments the functions take (see the second sentence on page 246), but fails to teach creating and initializing a new interpreter. However, Interp Manual teaches that the Tcl language contains a built-in function (interp command) that allows for the creation of a new interpreter (see "interp create" description on page 3 of Interp Manual) and the definition of new functions (see the third form of "interp alias" beginning at the bottom of page 2 and continuing onto page 3 of Interp Manual). Therefore, it would have been obvious to one having ordinary skill in the computer art at the time the invention was made to implement a $tclInit function in the Steinmetz method using the built-in Tcl commands as once taught by Interp Manual into the custom function scheme taught by ModelSim. One would be motivated to do so because ModelSim expressly supports and encourages this.

As per claims 14-16, Interp Manual further teaches a $tclExec function (interp eval; see page 3) that launches (evaluates) a new script and returns when an error occurs or when the script ends. The new script further accesses arguments that were passed to the extended Tcl function (interp eval). Therefore, in light of the above arguments, it would have been obvious to one having ordinary skill in the computer art at the time the invention was made to implement

$tclExec and $tclGetArgs functions in the Steinmetz method using the built-in Tcl commands as once taught by Interp Manual into the custom function scheme taught by ModelSim. One would be motivated to do so because ModelSim expressly supports and encourages this.

As per claim 17, Interp Manual further teaches a $tclClose function (interp delete; see page 3) that destroys (deletes) a Tcl interpreter and frees associated resources. Therefore, in light of the above arguments, it would have been obvious to one having ordinary skill in the computer art at the time the invention was made to implement a $tclClose function in the Steinmetz method using the built-in Tcl commands as once taught by Interp Manual into the custom function scheme taught by ModelSim. One would be motivated to do so because ModelSim expressly supports and encourages this.

As per claims 40-45, these are apparatus versions of the claimed methods discussed above (claims 12-17, respectively), wherein all claim limitations also have been addressed as set forth above. Thus, accordingly such claims also would have been obvious.

14. Claims 20 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steinmetz in view of ModelSim as applied to claim 11 above, and further in view of "Tcl Built-In Commands – error manual page" by Critchlow, Jr. (hereinafter Error Manual).

As per claim 20, in addition to the rationale provided in item 14 above, Error Manual further teaches a $tclSetErrorReg function (error) that allows a user to identify one register (errorInfo) in a Verilog simulation tat is linked to any error occurring in any interpreter. Therefore, in light of the above arguments, it would have been obvious to one having ordinary skill in the computer art at the time the invention was made to implement a $tclSetErrorReg

function in the Steinmetz method using the built-in Tcl commands as once taught by Error Manual into the custom function scheme taught by ModelSim. One would be motivated to do so because ModelSim expressly supports and encourages this.

As per claim 48, this is an apparatus version of the claimed method discussed above (claim 20), wherein all claim limitations also have been addressed as set forth above. Thus, accordingly such a claim also would have been obvious.

15. Claims 19 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steinmetz in view of ModelSim as applied to claim 11 above, and further in view of IEEE Standard 1364-1995 "IEEE standard hardware description language based on the Verilog hardware description language" (hereinafter Verilog Standard).

As per claim 19, in addition to the teachings applied above in item 13, Verilog Standard teaches functions ($fopen and $fdisplay) for allowing access to multi-channel descriptors, thereby allowing redirecting messages to log files that record messages directly from the simulation (see section 14.2.2 File output system tasks on pages 181 and 182). Therefore, it would have been obvious to one having ordinary skill in the computer art at the time the invention was made to further modify the method of Steinmetz to include functions that allow access to multi-channel descriptors as inherent in the Verilog language. One would be motivated to do so to add comments to automatically generated log files.

As per claim 47, this is an apparatus version of the claimed method discussed above (claim 19), wherein all claim limitations also have been addressed as set forth above. Thus, accordingly such a claim also would have been obvious.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Kiss whose telephone number is (703) 305-7737. The examiner can normally be reached on Tue. - Fri., 7:30 am - 5:00 pm. The examiner can also be reached on alternate Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory Morse can be reached on (703) 308-4789.

Any response to this action should be mailed to:
Commissioner of Patents and Trademarks
Washington, DC 20231
Or faxed to:
(703) 746-7239 (for formal communications intended for entry)
Or:
(703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")
Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, 22202, Fourth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

EBK
September 9, 2002

TUAN Q. DAM
PRIMARY EXAMINER